10026966.052402

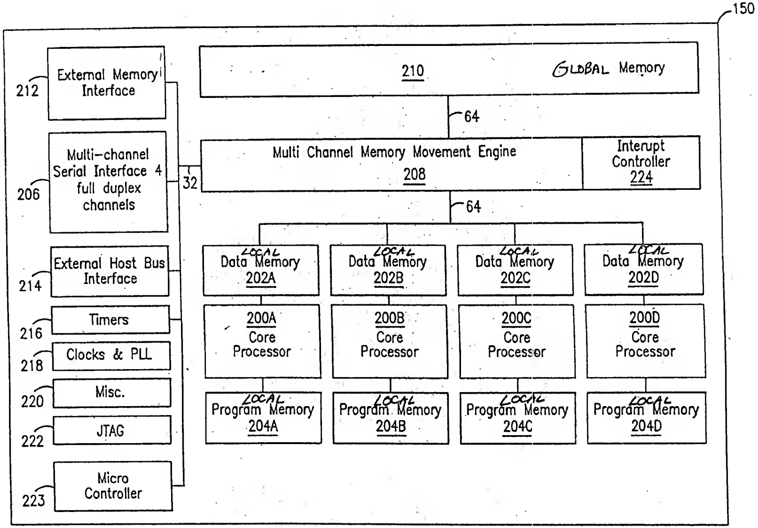

FIG. 1

10076955.052402

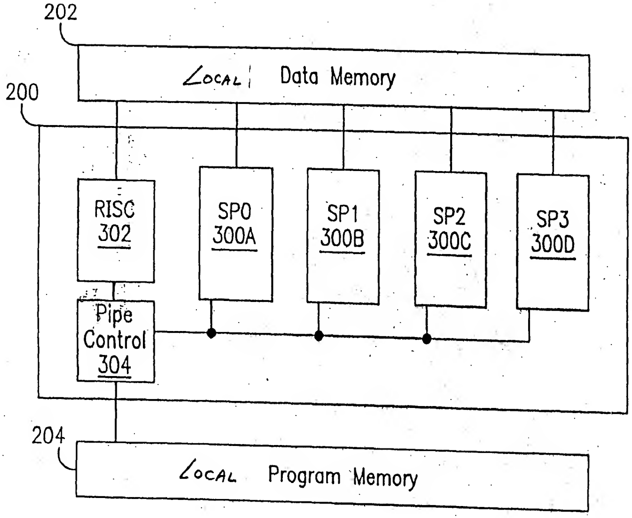

FIG. 2

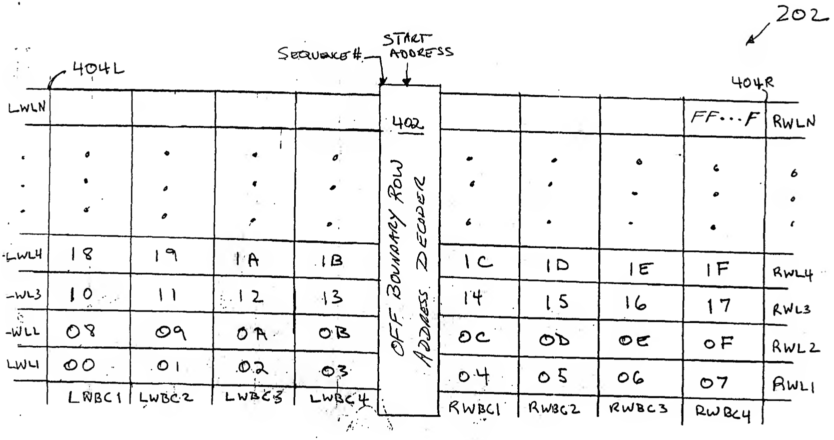
202
404L
SEQUENCE #
START ADDRESS
404R
402
OFF BOUNDARY ROW ADDRESS DECODER
LWLN
LWL4
WL3
WL2
LWL1
RWLN
RWL4
RWL3
RWL2
RWL1
FF...F
18
19
1A
1B
1C
1D
1E
1F
10
11
12
13
14
15
16
17
08
09
0A
0B
0C
0D
0E
0F
00
01
02
03
04
05
06
07
LWBC1
LWBC2
LWBC3
LWBC4
RWBC1
RWBC2
RWBC3
RWBC4

FIG. 3A

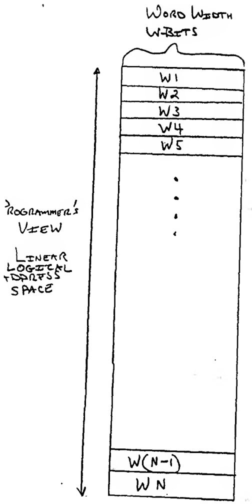
WORD WIDTH
W-BITS
W1
W2
W3
W4
W5
W(N-1)
WN
PROGRAMMER'S VIEW
LINEAR LOGICAL ADDRESS SPACE

FIG. 3B

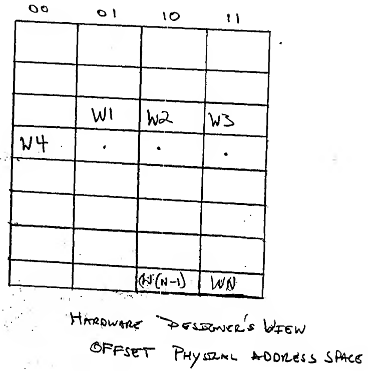
00
01
10
11
W1
W2
W3
W4
W(N-1)
WN
HARDWARE DESIGNER'S VIEW
OFFSET PHYSICAL ADDRESS SPACE

FIG. 3C

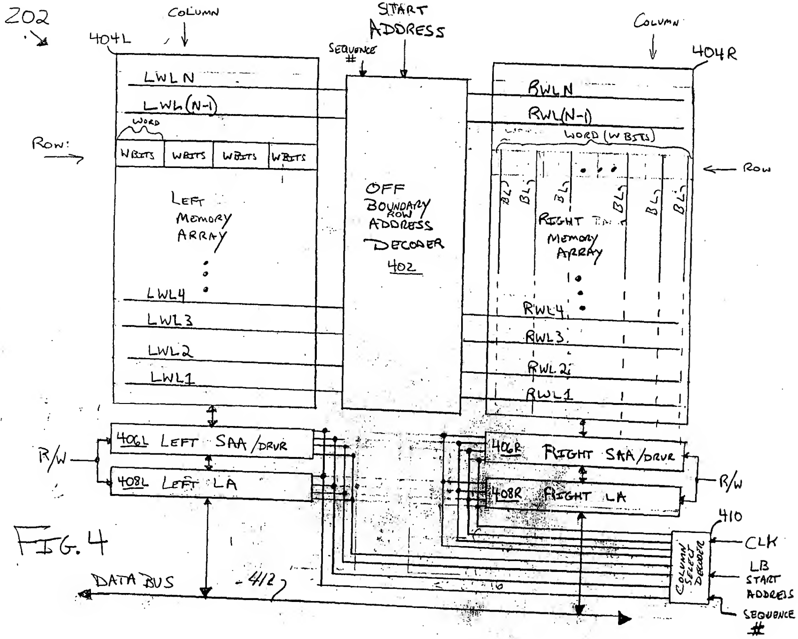
202
COLUMN
404L
START ADDRESS
SEQUENCE #
COLUMN
404R
LWL N
LWL(N-1)
WORD
ROW:
WBITS
WBITS
WBITS
WBITS
LEFT MEMORY ARRAY
LWL4
LWL3
LWL2
LWL1
OFF BOUNDARY ROW ADDRESS DECODER 402
RWL N
RWL(N-1)
WORD (W BITS)
ROW
BL
BL
BL
BL
BL
BL
RIGHT MEMORY ARRAY
RWL4
RWL3
RWL2
RWL1
406L LEFT SAA/DRVR
408L LEFT LA
R/W
406R RIGHT SAA/DRVR
408R RIGHT LA
R/W
410
COLUMN SELECT DECODER
CLK
LB START ADDRESS
SEQUENCE #
DATA BUS
412

FIG. 4

10076966 .052402

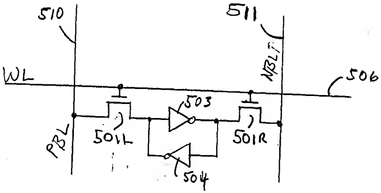

FIG. 5A

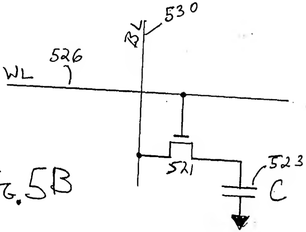

FIG. 5B

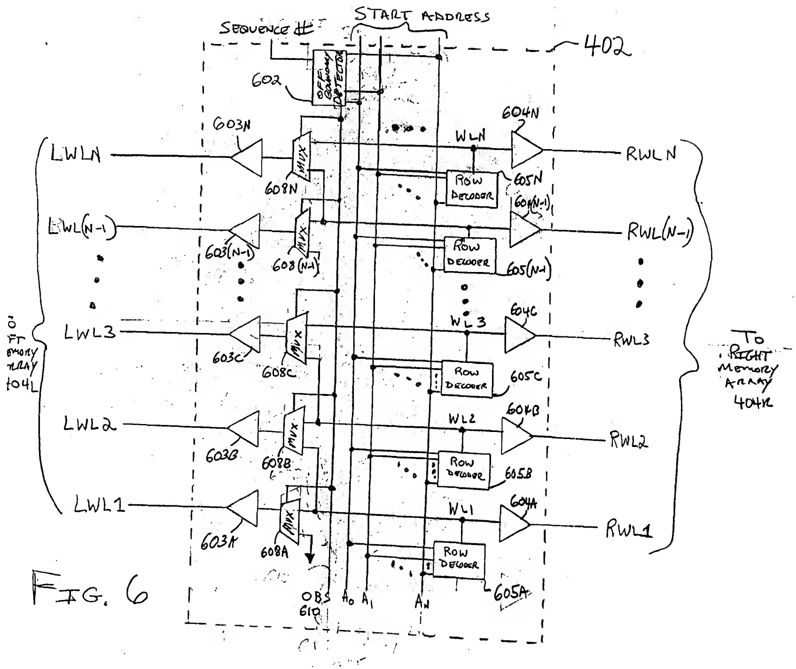
SEQUENCE #
START ADDRESS
402
602
OFF BOUNDARY DETECTOR
603N
604N
WLN
LWLN
RWL N
608N
605N
ROW DECODER
LWL(N-1)
RWL(N-1)
604(N-1)
603(N-1)
608(N-1)
605(N-1)
LWL3
RWL3
WL3
604C
603C
608C
605C
LWL2
RWL2
WL2
604B
603B
608B
605B
LWL1
RWL1
WL1
604A
603A
608A
605A
MUX
OBS
610
A0
A1
AN
To LEFT MEMORY ARRAY 404L
To RIGHT MEMORY ARRAY 404R

FIG. 6